REMARKS

Claims 1-31 are pending. Claims 32-93 are withdrawn from consideration. Independent claims 1, 18, and 25 were rejected under 35 U.S.C. 112(2) as being unclear. Independent claims 1, 18, and 25 were rejected under 35 U.S.C. 102(b) as being anticipated by Rhim (6,006,022).

The Examiner rejected independent claims 1, 18, and 25 under 35 U.S.C. 112(2) as being unclear. More specifically, the Examiner argued that the phrases "first parameter information" and "second parameter information" are unclear on what they refer to. The Applicants respectfully disagree. The specification gives guidance and numerous examples on what "first parameter information" and "second parameter information" refer to. In one example, "An input stage 101 receives selection and parameter information typically from a user about a processor core 102 and a peripheral 104 to be implemented on a programmable chip." (Page 11, Lines 3-5) In another example, "the generator program 105 can identify the parameters of the selected processor core 112 and peripheral 114 to generate a logic description with information for implementing the various modules." (Page 11, Lines 26-28) In still another example, "Figure 3C is a wizard page allowing a user to parameterize a Nios processor core. The user can select a 32-bit or a 16-bit architecture." (Page 15, Lines 19-21) In yet another example, "parameter information associated with the modules may indicate that the RISC processor core is 16-bit, the UART has a baud rate of 115,200bps, and the timer is a 4-bit timer." (Page 18, Lines 2-4) Consequently, this rejection is believed overcome.

The Examiner rejected independent claims 1, 18, and 25 under 35 U.S.C. 102(b) as being anticipated by Rhim. Rhim "allows the user to create a simulated software model 200, a real-time emulation of the target system via hardware model 100, as well as combined co-development environment 03 which uses both hardware model 100 and software model 200 together." (Column 14, Lines 21-25)

By contrast, the independent claims 1, 18, 25, and 31 recite "identifying first parameter information corresponding to a processor core" and identifying "second parameter information corresponding to a peripheral." Rhim does not teach or suggest identifying parameter information associated with a processor core or a peripheral. Rhim only mentions parameters in one paragraph in Column 16. Rhim states "there are parameters which need to be set in software model 200." (Column 16, Lines 19-20). Rhim uses parameters "to see if transitory disagreement

can be ignored and synchronization reached at the point of hardware halt." (Column 16, Lines 55-60). Rhim does not teach or suggest parameter information corresponding to a processor core or a peripheral as recited in the independent claims. Rhim only describes parameters associated with a "software model" and "synchronization."

The independent claims also recite "parameter information for configuring a processor core on a programmable chip" and "parameter information for configuring a peripheral on a programmable chip." Rhim makes no mention of parameter information for configuring a processor core or a peripheral.

The independent claims further recite generating a logic description "using the first and second parameter information." Rhim similarly makes no mention anywhere of generating a logic description "using the first and second parameter information."

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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54. (Withdrawn) A method for implementing a custom peripheral on a programmable logic device, the method comprising:

receiving first information associated with a custom peripheral;

receiving second information associated with a processor core;

generating a logic description using the first and second information to allow implementation of the custom peripheral on the programmable logic device.

55. (Withdrawn) The method of claim 54, wherein the custom peripheral is a custom peripheral component.

56. (Withdrawn) The method of claim 54, wherein the custom peripheral is a custom peripheral interface.

57. (Withdrawn) The method of claim 54, wherein the logic description is a synthesizable logic file.

58. (Withdrawn) The method of claim 57, wherein the logic description is an HDL file.

59. (Withdrawn) The method of claim 54, wherein the logic description is a synthesized logic file.

60. (Withdrawn) The method of claim 59, wherein the logic description is an EDF file.

61. (Withdrawn) A system for implementing a custom peripheral on a programmable logic device, the system comprising:

means for receiving first information associated with a custom peripheral;

means for receiving second information associated with a processor core;

means for generating a logic description using the first and second information to allow implementation of the custom peripheral on the programmable logic device.

62. (Withdrawn) The system of claim 61, wherein the custom peripheral is a custom peripheral component.

63. (Withdrawn) The system of claim 61, wherein the custom peripheral is a custom peripheral interface.

64. (Withdrawn) The system of claim 61, wherein the logic description is a synthesizable logic file.

65. (Withdrawn) The system of claim 64, wherein the logic description is an HDL file.

66. (Withdrawn) The system of claim 61, wherein the logic description is a synthesized logic file.